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DATE: Wednesday, April 06, 2005   [Printable Copy](#)   [Create Case](#)

<u>Set</u> <u>Name</u> side by side	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>			
<u>L2</u>	710/5,100,300,303,305;361/718,764,783;712/32-35;370/257,522,912;340/286.01;711/111.ccls.	8146	<u>L2</u>
<i>DB=DWPI; PLUR=YES; OP=OR</i>			
<u>L1</u>	710/5,100,300,303,305;361/718,764,783;712/32-35;370/257,522,912;340/286.01;711/111.ccls.	0	<u>L1</u>

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Terms	Documents
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Search:

L7





### Search History

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<u>L7</u>	L2 and L6	2	<u>L7</u>
<u>L6</u>	L3 same function	36	<u>L6</u>
<u>L5</u>	L4	11	<u>L5</u>
<u>L4</u>	L3 near10 function	11	<u>L4</u>
<u>L3</u>	(combin\$3 or adding) near5 plural\$3 near5 signal near5 "single"	532	<u>L3</u>
<u>L2</u>	710/5,100,300,303,305;361/718,764,783;712/32-35;370/257,522,912;340/286.01;711/111.ccls.	8146	<u>L2</u>
<i>DB=DWPI; PLUR=YES; OP=OR</i>			
<u>L1</u>	710/5,100,300,303,305;361/718,764,783;712/32-35;370/257,522,912;340/286.01;711/111.ccls.	0	<u>L1</u>

END OF SEARCH HISTORY

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L1: (350) (combin\$3 or adding)

L2: (8) 11 near10 function

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Default operator: OR

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BRS form

ISIR form

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1	BRS	L1	350	(combin\$3 or adding) near5 plural\$3 near5 signal	USPAT	2005/04/05 14:04			
2	BRS	L2	8	11 near10 function	USPAT	2005/04/05 14:06			

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IEEE JNL IEEE Journal or  
Magazine

IEE JNL IEE Journal or  
Magazine

IEEE  
CNF IEEE Conference  
Proceeding

IEE CNF IEE Conference  
Proceeding

IEEE  
STD IEEE Standard

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Results for "( combin\*&lt;in&gt;metadata ) &lt;and&gt; ( plural\*&lt;in&gt;metadata ) &lt;and&gt; ( single&lt;in&gt;metadata )"

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IEEE JNL IEEE Journal or Magazine

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IEE JNL IEE Journal or Magazine

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IEEE CNF IEEE Conference Proceeding

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IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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| <input type="checkbox"/> | <b>1. Design of low-distortion HF transmitter with power MOSFETs</b><br>Tozawa, Y.;<br>HF Radio Systems and Techniques, 1991., Fifth International Conference on<br>22-25 Jul 1991 Page(s):316 - 320<br><a href="#">AbstractPlus</a>   Full Text: <a href="#">PDF(328 KB)</a> IEE CNF   |
| <input type="checkbox"/> | <b>2. A new diagnostic test for operating margin problems in LSI memory</b><br>Hamaguchi, S.; Ishikawa, K.;<br>Solid-State Circuits, IEEE Journal of<br>Volume 18, Issue 4, Aug 1983 Page(s):409 - 413<br><a href="#">AbstractPlus</a>   Full Text: <a href="#">PDF(768 KB)</a> IEEE JNL  |
| <input type="checkbox"/> | <b>3. Space time transmit site diversity for OFDM multi base station system</b><br>Inoue, M.; Nakagawa, M.;<br>Mobile and Wireless Communications Network, 2002. 4th International Workshop on<br>9-11 Sept. 2002 Page(s):30 - 34<br><a href="#">AbstractPlus</a>   Full Text: <a href="#">PDF(347 KB)</a> IEEE CNF                 |
| <input type="checkbox"/> | <b>4. Video orbits of the projective group a simple approach to featureless estimation</b><br>Mann, S.; Picard, R.W.;<br>Image Processing, IEEE Transactions on<br>Volume 6, Issue 9, Sept. 1997 Page(s):1281 - 1295<br><a href="#">AbstractPlus</a>   <a href="#">References</a>   Full Text: <a href="#">PDF(484 KB)</a> IEEE JNL |
| <input type="checkbox"/> | <b>5. Construction of quasi-binary relations in the semantic networks</b><br>Zhilyakova, L.Yu.;<br>Artificial Intelligence Systems, 2002. (ICAIS 2002). 2002 IEEE International Conference<br>5-10 Sept. 2002 Page(s):24 - 25<br><a href="#">AbstractPlus</a>   Full Text: <a href="#">PDF(224 KB)</a> IEEE CNF                     |

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# Design of low-distortion HF transmitter with power MOSFETs

Tozawa, Y.  
Japan Radio Co. Ltd., Tokyo

This paper appears in: **HF Radio Systems and Techniques, 1991., Fifth International Conference on**  
Publication Date: 22-25 Jul 1991

On page(s): 316 - 320  
Meeting Date: 07/22/1991 - 07/25/1991  
Location: Edinburgh  
INSPEC Accession Number: 4000633  
Posted online: 2002-08-06 18:01:09.0

**Abstract**  
A 2-kW, 3-kW, 5-kW and 10-kW HF transmitter has been developed using the newest power MOSFETs in its final device and a single-ended push-pull (SEPP) circuit. The transmitter combines the output powers from a plurality of power amplifier (PA) modules to obtain a low-distortion output power

**Index Terms**  
**Inspec**

**Controlled Indexing**  
10 kW 2 kW 3 kW 5 kW insulated gate field effect transistors low-distortion HF  
transmitter power MOSFETs power transistors radio transmitters single ended push-pull  
circuit

**Non-controlled Indexing**  
10 kW 2 kW 3 kW 5 kW insulated gate field effect transistors low-distortion HF  
transmitter power MOSFETs power transistors radio transmitters single ended push-pull  
circuit

**Author Keywords**  
Not Available

**References**

No references available on IEEE Xplore.

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L7: Entry 1 of 2

File: PGPB

Dec 30, 2004

PGPUB-DOCUMENT-NUMBER: 20040268003

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040268003 A1

TITLE: Method and apparatus for providing signal functionality

PUBLICATION-DATE: December 30, 2004

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Nicholas, Ken	Tomball	TX	US	

APPL-NO: 10/ 602518 [PALM]

DATE FILED: June 24, 2003

INT-CL: [07] G06 F 13/00

US-CL-PUBLISHED: 710/303; 710/305

US-CL-CURRENT: 710/303; 710/305

REPRESENTATIVE-FIGURES: 3

## ABSTRACT:

A control circuit is adapted to receive a plurality of signals, each of the plurality of signals adapted to perform a separate respective function, and to combine the plurality of signals into a single signal adapted to perform each of the separate respective functions. For example, a device having a first type of processor is adapted to produce a plurality of signals, wherein each of the plurality of signals is produced for a different purpose, and having a circuit adapted to combine the plurality of signals into a single signal adapted to accomplish each different purpose. A coupling device is adapted to connect the device to another device, the coupling device having a connector adapted to receive the single signal but not the plurality of signals.

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L7: Entry 2 of 2

File: USPT

Mar 22, 1994

US-PAT-NO: 5297146

DOCUMENT-IDENTIFIER: US 5297146 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Communication terminal apparatus and its control method

DATE-ISSUED: March 22, 1994

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ogawa; Fukushige	Hino			JP

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Kabushiki Kaisha Toshiba	Kawasaki			JP	03

APPL-NO: 07/ 846988 [\[PALM\]](#)

DATE FILED: March 9, 1992

## PARENT-CASE:

This application is a continuation of application Ser. No. 07/586,387, filed Sep. 20, 1990, abandoned, which was a continuation of application Ser. No. 07/372,089, filed Jun. 27, 1989, abandoned.

## FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	63-165661	July 1, 1988
JP	63-165662	July 1, 1988
JP	63-165663	July 1, 1988

INT-CL: [05] H04J 3/12

US-CL-ISSUED: 370/110.1; 370/62, 379/67, 379/96, 379/100, 379/206

US-CL-CURRENT: [370/522](#); [370/271](#), [379/100.12](#), [379/206.01](#), [379/88.13](#), [379/93.17](#)

PRIOR-ART-DISCLOSED:

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PATENTEE-NAME

US-CL

<input type="checkbox"/>	<u>4672662</u>	June 1987	Nishino et al.	370/58.1
<input type="checkbox"/>	<u>4722082</u>	January 1988	Furuya et al.	370/110.1
<input type="checkbox"/>	<u>4723273</u>	February 1988	Diesel et al.	379/210
<input type="checkbox"/>	<u>4782510</u>	September 1988	Szlam	379/88
<input type="checkbox"/>	<u>4825461</u>	April 1989	Kurita et al.	379/100
<input type="checkbox"/>	<u>4831618</u>	May 1989	Bruce	370/62
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<input type="checkbox"/>	<u>4878240</u>	October 1989	Lin et al.	379/67
<input type="checkbox"/>	<u>4935955</u>	June 1990	Neudorfer	379/100
<input type="checkbox"/>	<u>4961185</u>	October 1990	Sawada	379/100

## FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0337610	March 1989	EP	379/100
0313313	April 1989	EP	
0357427	March 1990	EP	
1-190006	November 1989	JP	

## OTHER PUBLICATIONS

Duc, "ISDN Terminals and Integrated Services Delivery", IEEE Journal on Selected Areas in Communications, vol. SAC-4, No. 8, Nov. 1986, pp. 1188-1192.  
Swart, "ISDN Business Services", ICC '86, Session 1, Paper 4, vol. 1, Jun. 22, 1986, pp. 1-5.

ART-UNIT: 263

PRIMARY-EXAMINER: Olms; Douglas W.

ASSISTANT-EXAMINER: Kizou; Hassan

ATTY-AGENT-FIRM: Finnegan, Henderson, Farabow, Garrett &amp; Dunner

## ABSTRACT:

A communication terminal apparatus and its control method which allow the parallel execution of a plurality of communications with use of a plurality of data channels. The terminal apparatus comprises an image main controller and a voice main controller which can be operated independently of each other, two network controllers operated as associated with the operations of these image and voice main controllers respectively, two image transmission control circuits which are operated independently of each other, and an image file capable of storing image and voice data, thereby realizing the simultaneous execution of image and image communications and the simultaneous execution of voice and voice communications on a duplex communication basis.

20 Claims, 10 Drawing figures

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L4: Entry 1 of 11

File: PGPB

Dec 30, 2004

PGPUB-DOCUMENT-NUMBER: 20040268003

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040268003 A1

TITLE: Method and apparatus for providing signal functionality

PUBLICATION-DATE: December 30, 2004

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Nicholas, Ken	Tomball	TX	US	

US-CL-CURRENT: [710/303](#); [710/305](#)

## ABSTRACT:

A control circuit is adapted to receive a plurality of signals, each of the plurality of signals adapted to perform a separate respective function, and to combine the plurality of signals into a single signal adapted to perform each of the separate respective functions. For example, a device having a first type of processor is adapted to produce a plurality of signals, wherein each of the plurality of signals is produced for a different purpose, and having a circuit adapted to combine the plurality of signals into a single signal adapted to accomplish each different purpose. A coupling device is adapted to connect the device to another device, the coupling device having a connector adapted to receive the single signal but not the plurality of signals.

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File: PGPB

Dec 30, 2004

PGPUB-DOCUMENT-NUMBER: 20040268003

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040268003 A1

TITLE: Method and apparatus for providing signal functionality

PUBLICATION-DATE: December 30, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Nicholas, Ken	Tomball	TX	US	

US-CL-CURRENT: 710/303; 710/305

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 2. Document ID: US 6449066 B1

L4: Entry 2 of 11

File: USPT

Sep 10, 2002

US-PAT-NO: 6449066

DOCUMENT-IDENTIFIER: US 6449066 B1

TITLE: Polarization insensitive, high dispersion optical element

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 3. Document ID: US 6254551 B1

L4: Entry 3 of 11

File: USPT

Jul 3, 2001

US-PAT-NO: 6254551

DOCUMENT-IDENTIFIER: US 6254551 B1

TITLE: Apparatus for monitoring a mechanically transmitted signal based on the organs or vital functions and for processing the results

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 4. Document ID: US 6100929 A

L4: Entry 4 of 11

File: USPT

Aug 8, 2000

US-PAT-NO: 6100929

DOCUMENT-IDENTIFIER: US 6100929 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Image-taking system in which a high resolution image having suppressed color moire is obtained

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 5. Document ID: US 5297146 A

L4: Entry 5 of 11

File: USPT

Mar 22, 1994

US-PAT-NO: 5297146

DOCUMENT-IDENTIFIER: US 5297146 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Communication terminal apparatus and its control method

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 6. Document ID: US 5208792 A

L4: Entry 6 of 11

File: USPT

May 4, 1993

US-PAT-NO: 5208792

DOCUMENT-IDENTIFIER: US 5208792 A

TITLE: Recording and reproducing apparatus using opto-magneto media

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 7. Document ID: US 5107224 A

L4: Entry 7 of 11

File: USPT

Apr 21, 1992

US-PAT-NO: 5107224

DOCUMENT-IDENTIFIER: US 5107224 A

TITLE: Wideband single-ended voltage-to-current converter and gain-control circuit

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 8. Document ID: US 5045723 A

L4: Entry 8 of 11

File: USPT

Sep 3, 1991

US-PAT-NO: 5045723

DOCUMENT-IDENTIFIER: US 5045723 A

TITLE: Multiple input CMOS logic circuits

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 9. Document ID: US 4208916 A

L4: Entry 9 of 11

File: USPT

Jun 24, 1980

US-PAT-NO: 4208916

DOCUMENT-IDENTIFIER: US 4208916 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Electronic ultrasonic sector scanning apparatus and method

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 10. Document ID: US 3462547 A

L4: Entry 10 of 11

File: USOC

Aug 19, 1969

US-PAT-NO: 3462547

DOCUMENT-IDENTIFIER: US 3462547 A

TITLE: DATA PROCESSING SYSTEM FOR SIGNALS OBTAINED FROM A VIDEO SCANNER

DATE-ISSUED: August 19, 1969

INVENTOR-NAME: MACOVSKI ALBERT

US-CL-CURRENT: 348/571; 348/384.1

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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Terms	Documents
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L4: Entry 3 of 11

File: USPT

Jul 3, 2001

DOCUMENT-IDENTIFIER: US 6254551 B1

TITLE: Apparatus for monitoring a mechanically transmitted signal based on the organs or vital functions and for processing the results

Brief Summary Text (8):

In accordance with the invention, the composite signal spectrum generated by the sensor arrangement comprises said signals based on a plurality of different vital functions as a single combined signal. Thus the sensor arrangement generates a signal in which all the signals of different origins are incorporated in one signal spectrum. If the sensor arrangement is incorporated in a band fitted onto the user's chest, it may preferably comprise an acceleration transducer, a strain-gage sensor and an EMF diaphragm sensor. The capacitive acceleration transducer with high sensitivity both at low and high frequencies collects information on several different factors, such as movement, position and heart beat of a human being. On the other hand, from the EMF diaphragm sensor, whose electrical conductivity changes in response to pressure, information is obtained both on heart beat and respiration. The strain-gage sensor for its part gives information mainly on respiration. Particularly with regard to respiration, various coughs and even minor vibrations, such as rate of lungs or bronchi or a similar noise audible by means of a stethoscope, can be detected. The sensor arrangement also reacts to a variety of other functions, such as speech and blowing of the nose.

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L4: Entry 3 of 11

File: USPT

Jul 3, 2001

US-PAT-NO: 6254551

DOCUMENT-IDENTIFIER: US 6254551 B1

TITLE: Apparatus for monitoring a mechanically transmitted signal based on the organs or vital functions and for processing the results

DATE-ISSUED: July 3, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Varis; Reijo	Helsinki			FI

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Instrumentarium Corp.	Helsinki			FI	03

APPL-NO: 09/ 355576 [\[PALM\]](#)

DATE FILED: July 29, 1999

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
FI	970491	February 5, 1997
FI	970537	February 7, 1997

PCT-DATA:

APPL-NO	DATE-FILED	PUB-NO	PUB-DATE	371-DATE	102(E)-DATE
PCT/FI98/00107	February 5, 1998	W098/34540	Aug 13, 1998	Jul 29, 1999	Jul 29, 1999

INT-CL: [07] [A61](#) [B](#) [5/103](#)

US-CL-ISSUED: 600/595; 600/534

US-CL-CURRENT: [600/595](#); [600/534](#)

FIELD-OF-SEARCH: 600/534, 600/535, 600/538, 600/546, 600/390, 600/391, 600/587, 600/595

PRIOR-ART-DISCLOSED:

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<input type="checkbox"/>	<u>4474185</u>	October 1984	Diamond	
<input type="checkbox"/>	<u>4657026</u>	April 1987	Tagg	
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<input type="checkbox"/>	<u>5511553</u>	April 1996	Segalowitz	
<input type="checkbox"/>	<u>5515865</u>	May 1996	Scanlon	

## FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
44 37 538	May 1995	DE	
934012	March 1995	FI	
96/03075	February 1996	FR	
86/04497	August 1986	WO	
96/36279	November 1996	WO	

ART-UNIT: 376

PRIMARY-EXAMINER: Lacyk; John P.

ASSISTANT-EXAMINER: Wingood; Pamela

ATTY-AGENT-FIRM: Andrus, Scealess, Starke &amp; Sawall, LLP

## ABSTRACT:

The invention relates to an apparatus for monitoring a mechanically transmitted signal based on the organs or vital functions and for processing the results, the apparatus comprising a measuring sensor arrangement (10) comprising one or more measuring sensors (1) and signal processing means (2; 2, 3, 4) for processing the sensor signal(s), transmission means (5; 5a, 5b) for transmitting the signal generated by the sensor arrangement (10), a data collecting device (6) for receiving and storing the signal transmitted by the transmission means, means (7) for processing the signal stored by the data collecting device (6) and a display or output device (8) for presenting the results. In accordance with the invention the measuring sensor arrangement (10) is arranged to produce the signal spectra based on a plurality of vital functions as a single composite signal spectrum, and the means (7) for processing the information stored by the data collecting device (6) comprise processing software for dividing the signal spectrum generated by the measuring sensor arrangement into a plurality of partial spectra of different physiological origins.

15 Claims, 13 Drawing figures

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L4: Entry 4 of 11

File: USPT

Aug 8, 2000

DOCUMENT-IDENTIFIER: US 6100929 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Image-taking system in which a high resolution image having suppressed color moire is obtained

Brief Summary Text (16):

According to the present invention, a plurality of signals corresponding to images taken with different optical transfer functions by a solid-state imaging device is obtained, and the plurality of image signals are combined by a combining means to obtain a single high-resolution image having suppressed color moire.

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L4: Entry 4 of 11

File: USPT

Aug 8, 2000

US-PAT-NO: 6100929

DOCUMENT-IDENTIFIER: US 6100929 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Image-taking system in which a high resolution image having suppressed color moire is obtained

DATE-ISSUED: August 8, 2000

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ikeda; Masato	Higashikurume			JP
Sasaki; Takashi	Chigasaki			JP
Takeda; Nobuhiro	Kawasaki			JP

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Canon Kabushiki Kaisha	Tokyo			JP	03

APPL-NO: 08/ 731570 [PALM]

DATE FILED: October 16, 1996

## FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	7-272872	October 20, 1995

INT-CL: [07] H04 N 5/225, H04 N 9/68, H04 N 3/14

US-CL-ISSUED: 348/262; 348/219, 348/236, 348/273

US-CL-CURRENT: 348/262; 348/219.1, 348/236, 348/273

FIELD-OF-SEARCH: 348/234, 348/237, 348/241, 348/272, 348/273, 348/280, 348/262, 348/236, 348/259, 348/218, 348/219

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

Search Selected

Search ALL

Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>3911479</u>	October 1975	Sakurai	358/44
<input type="checkbox"/>	<u>4823186</u>	April 1989	Muramatsu	348/236

<input type="checkbox"/>	<u>4876591</u>	October 1989	Muramatsu	348/236
<input type="checkbox"/>	<u>4998164</u>	March 1991	Endo et al.	348/219
<input type="checkbox"/>	<u>5237363</u>	August 1993	Okada et al.	354/412
<input type="checkbox"/>	<u>5561460</u>	October 1996	Katoh et al.	348/219
<input type="checkbox"/>	<u>5737017</u>	April 1998	Udagawa et al.	348/273
<input type="checkbox"/>	<u>5745171</u>	April 1998	Ogawa et al.	348/273

## FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0272634	June 1988	EP	
0416876	March 1991	EP	
0522647	January 1993	EP	
4142892	May 1992	JP	
6189318	July 1994	JP	
250649	September 1994	JP	
1441553	July 1976	GB	

ART-UNIT: 272

PRIMARY-EXAMINER: Garber; Wendy

ASSISTANT-EXAMINER: Nguyen; Luong

ATTY-AGENT-FIRM: Fitzpatrick, Cella, Harper &amp; Scinto

## ABSTRACT:

First and second optical images of an object are respectively taken using two optical filters, having different optical transfer properties, which are placed one at a time in the optical path of the taken images. The first and second optical images are converted to first and second memories, respectively. The first digital signal indicative of the first optical image is provided to a luminance-signal generator which produces a luminance signal. The second digital signal indicative of the second optical image is provided to a color-signal generator which produces a color signal. A combining unit combines the luminance signal and the color signal to produce a single image signal of the object having a suppressed color moire. An image reproduction device receives the single image signal to reproduce the image of the object.

10 Claims, 19 Drawing figures

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L4: Entry 9 of 11

File: USPT

Jun 24, 1980

DOCUMENT-IDENTIFIER: US 4208916 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Electronic ultrasonic sector scanning apparatus and method

Brief Summary Text (20):

This delay circuitry, by dividing the impressed delay between first and second delay elements, enables separate control of the delay portions. This feature can enhance system economy by, for example, facilitating the use of relatively inexpensive delay elements to effect a first portion of constant time delay, restricting the use of more expensive variable delay elements to impression of those portions of time delay which must, in fact, be variable. Moreover, the combining of signals from a plurality of first delay elements for processing by a single second delay element obviously "dovetails" the function of each second delay element, reducing the number of such elements required.

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L4: Entry 9 of 11

File: USPT

Jun 24, 1980

US-PAT-NO: 4208916

DOCUMENT-IDENTIFIER: US 4208916 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Electronic ultrasonic sector scanning apparatus and method

DATE-ISSUED: June 24, 1980

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Thomenius; Kai E.	Durham	CT		
Bernardi; Richard B.	Cheshire	CT		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Picker Corporation	Cleveland	OH			02

APPL-NO: 05/ 941919 [PALM]

DATE FILED: September 13, 1978

INT-CL: [02] G01N 29/04

US-CL-ISSUED: 73/626; 73/628, 128/660

US-CL-CURRENT: 73/626; 600/447, 73/628

FIELD-OF-SEARCH: 73/626, 73/628, 73/611, 73/609, 128/660, 340/5MP

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

[Search Selected](#) [Search ALL](#) [Clear](#)

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>3166731</u>	January 1965	Joy	
<input type="checkbox"/>	<u>3373602</u>	March 1968	Wendt et al.	
<input type="checkbox"/>	<u>3723955</u>	March 1973	Lyons et al.	340/5R
<input type="checkbox"/>	<u>3875550</u>	April 1975	Quate et al.	340/5MP
<input type="checkbox"/>	<u>3924259</u>	December 1975	Butler et al.	340/5R
<input type="checkbox"/>	<u>4058003</u>	November 1977	Macovski	73/626
<input type="checkbox"/>	<u>4116229</u>	September 1978	Pering	73/626





4152678

May 1979

Shott et al.

73/619

## OTHER PUBLICATIONS

Von Ramm et al., Cardiac Imaging Using a Phased Array Ultrasound System, Circulation, vol. 53, No. 2, Feb. 1976, pp. 258-262.

ART-UNIT: 244

PRIMARY-EXAMINER: Ciarlante; Anthony V.

ATTY-AGENT-FIRM: Watts, Hoffmann, Fisher &amp; Heinke Co.

## ABSTRACT:

An electronically scanned phased array diagnostic system for describing internal structure of a subject by the use of ultrasonic energy. The system includes a transducer unit with an array of ultrasonic energy conversion segments and control circuitry for actuating the segments to direct ultrasonic energy into the subject. Imaging circuitry is included for interpreting electrical return signals produced by the segments in response to ultrasonic echoes. The imaging circuitry includes transmission delay circuits for imposing time delays on the return signals for steering and focusing system echo reception. Each transmission delay circuit includes first and second delay elements for impressing first and second delay time components on the return signals. Each pair of the first delay elements are coupled in parallel with separate transducer elements, and serially combined with a downstream second delay element.

The first delay elements provide a portion of the reception steering capability. The second elements provide the remainder of the steering, and the beam focusing, delay components. The system further includes display apparatus responsive to the delayed return signals for producing an image of the subjects internal structure.

17 Claims, 4 Drawing figures

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# United States Patent

Thomas et al.

(11) 4,208,916  
(45) Jun. 24, 1980

## [36] ELECTRONIC ULTRASONIC SECTOR SCANNING APPARATUS AND METHOD

[73] Inventors: Earl S. Thomas, Durham; Richard S. Bernard, Charlotte, both of Conn.

[75] Assignor: Fisher Corporation, Cleveland, Ohio

[21] Appl. No.: 841,919

[22] Filed: Sep. 12, 1979

[31] Int. Cl.: G01N 29/04

[32] U.S. Cl.: 73/626; 73/628; 121/660

[33] Field of Search: 73/626, 628, 611, 609; 121/660; 340/7.1 MP

### [34] References Cited

#### U.S. PATENT DOCUMENTS

3,158,731	1/1965	Jay
3,173,623	5/1968	Wash et al.
3,723,855	3/1973	Lynn et al.
3,973,330	4/1976	Quinn et al.
3,994,339	12/1976	Baker et al.
4,028,003	11/1977	Macquid
4,116,329	9/1978	Peting
4,192,678	3/1979	Shott et al.

#### OTHER PUBLICATIONS

Von Ramm et al., Cardiac Imaging Using a Phased Array Ultrasound System, *Circulation*, vol. 53, No. 2, Feb. 1976, pp. 230-343.

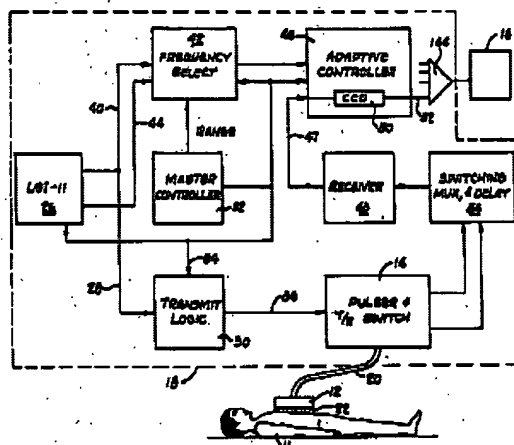
Primary Examiner—Anthony V. Cleburne  
Attorney Agent, or Firm—Watts, Hoffmann, Fisher & Hatcher Co.

### ABSTRACT

An electronically scanned phased array diagnostic system for describing internal structures of a subject by the use of ultrasonic energy. The system includes a transmitter unit with an array of ultrasonic energy conversion segments and control circuitry for sequencing the segments to direct ultrasonic energy into the subject. Imaging circuitry is included for intercepting electrical return signals produced by the segments in response to ultrasonic echoes. The imaging circuitry includes transmission delay circuits for imposing time delays on the return signals for steering and focusing system echo reception. Each transmission delay circuit includes first and second delay elements for imposing first and second delay time components on the return signals. Each pair of the first delay elements are coupled in parallel with separate transmitter elements, and serially combined with a downstream second delay element.

The first delay elements provide a portion of the reception steering capability. The second elements provide the remainder of the steering, and the beam focusing, delay components. The system further includes display apparatus responsive to the delayed return signals for producing an image of the subjects internal structure.

17 Claims, 4 Drawing Figures



# United States Patent (19)

Ogawa

(11) Patent Number: 5,297,146

(45) Date of Patent: Mar. 22, 1994

## COMMUNICATION TERMINAL APPARATUS AND ITS CONTROL METHOD

(75) Inventor: Fumihiko Ogawa, Hino, Japan  
(73) Assignee: Kabushiki Kaisha Toshiba, Kawasaki, Japan

(21) Appl. No.: 846,982

(22) Filed: Mar. 9, 1992

### Related U.S. Application Data

(63) Continuation of Ser. No. 584,387, Sep. 23, 1990, abandoned, which is a continuation of Ser. No. 772,089, Jun. 27, 1989, abandoned.

### Foreign Application Priority Data

Jul. 1, 1991 [JP] Japan 63-145661  
Jul. 1, 1991 [JP] Japan 63-145662  
Jul. 1, 1991 [JP] Japan 63-145663

(51) Int. Cl. H04M 3/12

(52) U.S. Cl. 379/67; 379/96; 379/100; 379/206

### References Cited

#### U.S. PATENT DOCUMENTS

4,672,662 6/1987 Nishino et al. 379/58.1  
4,722,082 1/1988 Furuya et al. 379/110.1  
4,722,373 2/1988 Diesel et al. 379/210  
4,722,510 6/1988 Sakai 379/58  
4,823,461 4/1989 Kozuka et al. 379/100  
4,831,611 5/1989 Bruce 379/62  
4,830,678 5/1989 Adachi 379/100  
4,874,340 10/1989 Lin et al. 379/67  
4,914,933 6/1990 Neudorfer 379/100  
4,911,133 10/1990 Swends 379/100

### FOREIGN PATENT DOCUMENTS

0337610 3/1989 European Pat. Off. 379/100  
0313313 4/1989 European Pat. Off.  
0337437 3/1990 European Pat. Off.  
1-190006 11/1989 Japan

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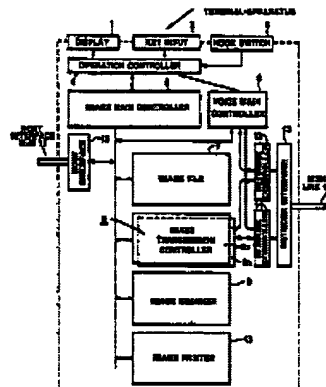
Doc. "ISDN Terminals and Integrated Service Delivery", IEEE Journal on Selected Areas in Communications, vol. SAC-4, No. 8, Nov. 1986, pp. 1182-1192.  
Swart, "ISDN Business Services", RCC '84, Session 1, Paper 4, vol. 1, Jun. 12, 1986, pp. 1-5.

Primary Examiner—Douglas W. Olms  
Assistant Examiner—Hossein Khatib  
Attorney, Agent, or Firm—Finnegan, Henderson, Farshaw, Garrett & Danner

### ABSTRACT

A communication terminal apparatus and its control method which allow the parallel execution of a plurality of communications with use of a plurality of data channels. The terminal apparatus comprises an image main controller and a voice main controller which can be operated independently of each other, two network controllers operated as associated with the operations of these image and voice main controllers respectively, two image transmission control circuits which are operated independently of each other, and an image file capable of storing image and voice data, thereby realizing the simultaneous execution of image and image communications and the simultaneous execution of voice and voice communications on a duplex communication basis.

20 Claims, 8 Drawing Sheets



US-PAT-NO: 5297146

DOCUMENT-IDENTIFIER: US 5297146 A

\*\*See image for Certificate of Correction\*\*

TITLE: Communication terminal apparatus and its control method

----- KWIC -----

Claims Text - CLTX (48):

wherein said voice control means includes switch means for outputting the voice signal inputted from a single voice input means to said plurality of network control means and for performing an adding function using the voice signal outputted from said plurality of network control means and outputting it to a single voice output means, whereby a conference speech is realized with a plurality of parties connected through said plurality of network control means.

# United States Patent (19)

Mao

(11) Patent Number: 5,045,723

(45) Date of Patent: Sep. 3, 1991

## (54) MULTIPLE INPUT CMOS LOGIC CIRCUIT

(73) Inventor: Robert S. Mao, San Jose, Calif.

(73) Assignee: International Business Machines Corporation, Armonk, N.Y.

(21) Appl. No.: 860,381

(22) Filed: Jul. 21, 1990

(31) Int. Cl. .... H03K 19/094

(52) U.S. Cl. .... 307/449; 307/279

(54) Field of Search .... 307/451, 449, 448, 445, 307/272.2, 279, 291

## (56) References Cited

### U.S. PATENT DOCUMENTS

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4,123,469	10/1978	Devine et al.	307/203
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### FOREIGN PATENT DOCUMENTS

1053099	10/1983	U.S.S.R.
1064443	12/1983	U.S.S.R.

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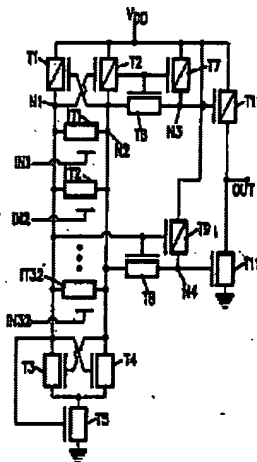
Abstract for 1053099, Soviet Union, English Translation.  
Abstract for 1064443, Soviet Union, English Translation.

Primary Examiner—David Hodspeith  
Assistant Examiner—Scott A. Ouellette  
Attorney, Agent, or Firm—Baker, Maxham, Jester & Moscor

## (57) ABSTRACT

A multiple input CMOS logic circuit includes a bistable input section with two nodes. In an inactive state, the input section maintains the nodes at opposite CMOS logic levels. In an active state, the nodes are maintained at substantially equal levels positioned between the two CMOS logic levels. The input circuit includes a set of parallel CMOS transistor pairs, cross connected at the nodes. The CMOS pairs are unbalanced by inequality of transistor gate widths. The imbalance causes the input circuit to assume the inactive state. A plurality of input CMOS transistors are connected in parallel between the nodes and receive input signals at their gates. When any of the input transistors is turned on by a change of input signal state, it conducts between the nodes, causing the input circuit to transition to the active state. An output buffer connected to the nodes translates the node levels to CMOS signal levels.

7 Claims, 2 Drawing Sheets



US-PAT-NO: 5045723

DOCUMENT-IDENTIFIER: US 5045723 A

Details view

TITLE: Multiple input CMOS logic circuits

----- KWIC -----

Detailed Description Text - DETX (19):

Contemplation of the CMOS logic circuits illustrated in FIGS. 3A, 5, and 6 will lead to the conclusion that the unbalanced, bistable CMOS input circuit can, when combined with an appropriate output buffer, accept a plurality of input logic signals, and combine those signals according to a CMOS logic function in a single circuit framework. Therefore, the invention permits the construction of single element, multiple input circuits in CMOS technology which can significantly reduce the count of circuit elements in the actual area occupied by the logic circuit for a very high number of inputs.

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L2: Entry 17 of 40

File: USPT

Sep 1, 1992

DOCUMENT-IDENTIFIER: US 5144543 A

TITLE: Domestic appliance having electrically isolated input control circuitry

Brief Summary Text (12):

In a preferred embodiment of the present invention, a single photo-electric isolator is located in a single signal transmission path. While plural signals may be necessary to control the power control circuit and its associated power components, the plural signals may be converted using a parallel-series converter into a serial combined signal for transmission on this single communication link. Similarly, the power control circuit is provided with a series-parallel converter to convert the information transmitted serially into parallel control signals for processing by the power control circuit to control the various power components. Alternatively, the teachings of the present invention may be utilized to transmit control pulses in parallel through the use of several isolated communication conductors between the input control circuit and power control circuit.

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L2: Entry 17 of 40

File: USPT

Sep 1, 1992

US-PAT-NO: 5144543

DOCUMENT-IDENTIFIER: US 5144543 A

TITLE: Domestic appliance having electrically isolated input control circuitry

DATE-ISSUED: September 1, 1992

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Striek; Ralf-Jurgen	Berlin			DE
Muller; Peter	Berlin			DE

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
The Coca-Cola Company	Atlanta	GA			02
Bosch-Siemens Hausgerate GmbH	Munich			DE	03

APPL-NO: 07/ 631959 [\[PALM\]](#)

DATE FILED: December 21, 1990

## FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
DE	3942430	December 21, 1989

INT-CL: [05] H02M 3/335

US-CL-ISSUED: 363/16; 363/50, 323/902

US-CL-CURRENT: [363/16](#); [323/902](#), [363/50](#)

FIELD-OF-SEARCH: 323/902, 323/904, 323/905, 323/909, 363/50, 363/125, 363/126, 363/15-16

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<a href="#">4384259</a>	May 1983	Capewell	323/902
<input type="checkbox"/>	<a href="#">4584519</a>	April 1986	Grvodis	323/905
<input type="checkbox"/>	<a href="#">4933825</a>	June 1990	Allington et al.	323/902



ART-UNIT: 212

PRIMARY-EXAMINER: Wong; Peter S.

ATTY-AGENT-FIRM: Birch, Stewart, Kolasch & Birch

ABSTRACT:

In a domestic appliance such as a washer, dishwasher, dryer, beverage preparation device or the like having several control circuits driven by varying voltage supplies, the input control circuit is supplied with a relatively low voltage and is electrically isolated from higher voltages within the circuitry of the appliance. An optical isolator is provided in the communication channel between the input control circuit and a power control circuit which is connected to circuit elements connected to the A.C. line voltage. The low voltage supply driving the input control circuit is also isolated from the A.C. line voltage. All operator accessible components are coupled to the input control circuit and are therefore isolated from the A.C. line voltage.

15 Claims, 2 Drawing figures

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L2: Entry 18 of 40

File: USPT

Mar 19, 1991

DOCUMENT-IDENTIFIER: US 5001398 A

TITLE: Lamp intensity control system having over-current protection

## CLAIMS:

6. A monolithically integrated lamp intensity control system which combines a plurality of signals into a single pulse width modulated signal for controlling the intensity in at least one lamp, comprising:

control signal encoder means coupled for receiving a tail light signal, a brake light signal, and a turn indicator signal for providing a decoded driver signal;

driver means coupled for receiving the decoded driver signal for providing a gate driver signal;

a SENSFET having a gate coupled for receiving the gate driver signal, a source coupled for receiving a first supply voltage, a first drain coupled to said at least one lamp, and having a second and third drain;

pulse width modulation means coupled to said control signal encoder means for modulating the decoded driver signal; and

temperature limit means located in proximity to said SENSFET and coupled to said driver means for turning off said driver means if the temperature detected by said temperature limit means exceeds a predetermined value, and for providing an over-temperature signal.

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L2: Entry 18 of 40

File: USPT

Mar 19, 1991

US-PAT-NO: 5001398

DOCUMENT-IDENTIFIER: US 5001398 A

TITLE: Lamp intensity control system having over-current protection

DATE-ISSUED: March 19, 1991

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dunn; William C.	Mesa	AZ		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Motorola, Inc.	Schaumburg	IL			02

APPL-NO: 07/ 374720 [\[PALM\]](#)

DATE FILED: July 3, 1989

INT-CL: [05] H60Q 1/26

US-CL-ISSUED: 315/77; 315/80, 315/291, 315/293, 315/309, 330/298, 340/468, 340/469, 307/10.8

US-CL-CURRENT: [315/77](#); [307/10.8](#), [315/291](#), [315/293](#), [315/309](#), [315/80](#), [330/298](#), [340/468](#), [340/469](#)

FIELD-OF-SEARCH: 315/77, 315/82, 315/119, 315/121, 315/291, 315/294, 315/292, 315/293, 315/312, 315/309, 340/475, 340/468, 340/469, 330/289, 330/298

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

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<input type="checkbox"/> <a href="#">1981985</a>	November 1934	Braselton	307/10.8
<input type="checkbox"/> <a href="#">3244934</a>	May 1966	Webb	340/469
<input type="checkbox"/> <a href="#">3277442</a>	October 1966	Kearny	340/469
<input type="checkbox"/> <a href="#">3284770</a>	November 1966	Bleiweiss et al.	340/475
<input type="checkbox"/> <a href="#">3603840</a>	September 1971	Durocher	315/82
<input type="checkbox"/> <a href="#">4149124</a>	April 1979	Glogolja	330/290
<input type="checkbox"/> <a href="#">4904906</a>	February 1990	Atherton et al.	315/291

ART-UNIT: 252

PRIMARY-EXAMINER: Laroche; Eugene R.

ASSISTANT-EXAMINER: Dinh; Son

ATTY-AGENT-FIRM: Bingham; Michael D. Atkins; Robert D.

ABSTRACT:

A lamp intensity control system combines the functions of the tail light, the brake light, and the turn indicator light signals into one signal for controlling a plurality of lamps in an automobile. The tail light, brake light and turn indicator light signals are combined into one signal and modulated wherein the percent of modulation determines the intensity of the brightness of the plurality of lamps. Temperature protection is provided wherein a temperature limit circuit monitors the temperature of a SENSFET and disables the SENSFET if its temperature exceeds a predetermined magnitude. Over-current and open lamp conditions are monitored by comparator circuits. An over-current condition causes the SENSFET to be disabled. An over-temperature, over-current or open-lamp condition is signaled by a fault output signal.

13 Claims, 2 Drawing figures

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L3: Entry 14 of 36

File: USPT

Mar 9, 1999

DOCUMENT-IDENTIFIER: US 5881250 A

TITLE: Host adapter system including an integrated PCI buffer controller and XOR function circuit

## CLAIMS:

1. A host adapter system comprising:

a secondary computer bus;

a plurality of an I/O buses;

a host adapter circuit wherein said host adapter circuit is connected to said secondary computer bus, and to said I/O bus;

an external buffer memory; and

an integrated circuit including a buffer controller and a data function circuit, said integrated circuit is connected to said secondary computer bus and to said external buffer memory wherein said external buffer memory is accessible to said host adapter circuit through said integrated circuit and further wherein said data function circuit receives a plurality of input signals, with at least one of said plurality of input signals being one of (a) data from said external buffer memory, and (b) data from said secondary computer bus, and combines said plurality of input signals to generate a single output signal that is written to said external buffer memory.

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L3: Entry 14 of 36

File: USPT

Mar 9, 1999

US-PAT-NO: 5881250

DOCUMENT-IDENTIFIER: US 5881250 A

TITLE: Host adapter system including an integrated PCI buffer controller and XOR function circuit

DATE-ISSUED: March 9, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Young; B. Arlen	Palo Alto	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Adaptec, Inc.	Milipitas	CA			02

APPL-NO: 08/ 615477 [\[PALM\]](#)

DATE FILED: March 15, 1996

INT-CL: [06] [G06 F 13/00](#)

US-CL-ISSUED: 395/281; 395/282, 395/309, 395/842

US-CL-CURRENT: [710/306](#); [710/22](#)

FIELD-OF-SEARCH: 395/250, 395/282, 395/439, 395/281, 395/285, 395/325, 395/275, 395/309, 395/825, 395/500, 395/800, 395/842

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

[Search Selected](#) [Search ALL](#) [Clear](#)

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> <a href="#">4373181</a>	February 1983	Chisholm et al.	395/421.01
<input type="checkbox"/> <a href="#">4468759</a>	August 1984	Kung et al.	365/201
<input type="checkbox"/> <a href="#">4965801</a>	October 1990	DuLac	
<input type="checkbox"/> <a href="#">5033048</a>	July 1991	Pierce et al.	371/21.2
<input type="checkbox"/> <a href="#">5070502</a>	December 1991	Supnik	371/11.1
<input type="checkbox"/> <a href="#">5131082</a>	July 1992	Bonevento et al.	395/275
<input type="checkbox"/> <a href="#">5251312</a>	October 1993	Sodos	395/425

<input type="checkbox"/>	<u>5278969</u>	January 1994	Pashan et al.	395/425
<input type="checkbox"/>	<u>5293624</u>	March 1994	Andrade et al.	395/425
<input type="checkbox"/>	<u>5373512</u>	December 1994	Brady	371/40.1
<input type="checkbox"/>	<u>5436912</u>	July 1995	Lustig	371/21.2
<input type="checkbox"/>	<u>5475814</u>	December 1995	Tomimitsu	395/183.06
<input type="checkbox"/>	<u>5553260</u>	September 1996	Miyane	395/421.1
<input type="checkbox"/>	<u>5555390</u>	September 1996	Judd et al.	
<input type="checkbox"/>	<u>5561772</u>	October 1996	Dornier et al.	395/281
<input type="checkbox"/>	<u>5586268</u>	December 1996	Chen et al.	
<input type="checkbox"/>	<u>5611057</u>	March 1997	Pecone et al.	
<input type="checkbox"/>	<u>5615383</u>	March 1997	Caudel et al.	395/800

ART-UNIT: 271

PRIMARY-EXAMINER: An; Meng-Ai T.

ASSISTANT-EXAMINER: Dharia; Rupal D.

ATTY-AGENT-FIRM: Gunnison; Forrest

ABSTRACT:

A host adapter system includes a secondary computer bus, a plurality of I/O buses, and a plurality of host adapter circuits. Each host adapter circuit is connected to the secondary computer bus and to one I/O bus in the plurality of I/O buses. An integrated buffer controller and data function circuit is connected to the secondary computer bus and an external buffer memory. The external buffer memory appears to the plurality of host adapter circuits as a host computer buffer memory. The integrated buffer controller and data function circuit includes a data function circuit that is controlled by addresses supplied to the circuit. The integrated buffer controller and data function circuit has a bus interface that is used to connect the circuit to the secondary computer bus. A data channel in the integrated buffer controller and data function circuit connects the bus interface to a buffer memory controller. The buffer memory controller has a buffer memory port that is connected to the external buffer memory. The integrated buffer controller and data function circuit includes a slave data channel and a master data channel.

11 Claims, 8 Drawing figures

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L3: Entry 19 of 36

File: USPT

Dec 20, 1994

DOCUMENT-IDENTIFIER: US 5375217 A

TITLE: Method and apparatus for synchronizing disk drive requests within a disk array

Abstract Text (1):

A simple method and circuit for qualifying and combining individual request signals received from a plurality of disk drives within a disk array to generate a single, synchronized request signal for the disk array. The circuit includes an activity register for storing a bit pattern which identifies those disk drives which are in use within the array. Each bit position within the activity corresponds to a different disk drive within the disk array. A logic one stored in a bit position identifies the disk drive corresponding to the bit position as being active while a logic zero stored in a bit position identifies the disk drive corresponding to the bit position as being inactive. The circuit further includes an OR gate associated with each disk drive within the disk array, each OR gate having a first input connected to receive the bit information corresponding to its associated disk drive from the activity register, and a second inverting input for receiving the individual request signal from its associated disk drive. The outputs of the OR gates are provided to an AND logic operator which combines the received signals to generate the request signal for the array. Additionally, the circuit includes a NAND gate associated with each disk drive within the disk array. Each NAND gate has a first input connected to receive the bit corresponding to its associated disk drive from the activity register, and a second input for receiving an acknowledge signal for the disk array. The NAND gates function to provide individual acknowledge signals to the active disk drives within the array.

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L3: Entry 19 of 36

File: USPT

Dec 20, 1994

US-PAT-NO: 5375217

DOCUMENT-IDENTIFIER: US 5375217 A

TITLE: Method and apparatus for synchronizing disk drive requests within a disk array

DATE-ISSUED: December 20, 1994

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Jibbe; Mahmoud K.	Wichita	KS		
McCombs; Craig C.	Wichita	KS		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
NCR Corporation	Dayton	OH			02

APPL-NO: 07/ 857539 [\[PALM\]](#)

DATE FILED: March 25, 1992

INT-CL: [05] G06F 13/00

US-CL-ISSUED: 395/425

US-CL-CURRENT: [711/114](#)

FIELD-OF-SEARCH: 395/425

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

Search Selected

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> <a href="#">4232366</a>	November 1980	Levy et al.	395/325
<input type="checkbox"/> <a href="#">4293908</a>	October 1981	Bradley et al.	395/275
<input type="checkbox"/> <a href="#">4423448</a>	December 1983	Frandsen	360/106
<input type="checkbox"/> <a href="#">4600990</a>	July 1986	Gershenson et al.	395/425
<input type="checkbox"/> <a href="#">5179704</a>	January 1993	Jibbe et al.	395/725

ART-UNIT: 232

PRIMARY-EXAMINER: Robertson; David L.

ATTY-AGENT-FIRM: Stover; James M.

## ABSTRACT:

A simple method and circuit for qualifying and combining individual request signals received from a plurality of disk drives within a disk array to generate a single, synchronized request signal for the disk array. The circuit includes an activity register for storing a bit pattern which identifies those disk drives which are in use within the array. Each bit position within the activity corresponds to a different disk drive within the disk array. A logic one stored in a bit position identifies the disk drive corresponding to the bit position as being active while a logic zero stored in a bit position identifies the disk drive corresponding to the bit position as being inactive. The circuit further includes an OR gate associated with each disk drive within the disk array, each OR gate having a first input connected to receive the bit information corresponding to its associated disk drive from the activity register, and a second inverting input for receiving the individual request signal from its associated disk drive. The outputs of the OR gates are provided to an AND logic operator which combines the received signals to generate the request signal for the array. Additionally, the circuit includes a NAND gate associated with each disk drive within the disk array. Each NAND gate has a first input connected to receive the bit corresponding to its associated disk drive from the activity register, and a second input for receiving an acknowledge signal for the disk array. The NAND gates function to provide individual acknowledge signals to the active disk drives within the array.

12 Claims, 7 Drawing figures

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L3: Entry 29 of 36

File: USPT

Feb 19, 1980

DOCUMENT-IDENTIFIER: US 4188708 A

TITLE: Integrated circuit package with optical input coupler

Brief Summary Text (14):

U.S. Pat. No. 3,423,594 issued Jan. 21, 1969 to A. G. Galopin, describes a photosensitive semiconductor device in which a plurality of fiber optic light rods are coupled to a light sensitive base portion of what is essentially a phototransistor. Combinations of light signals on the fiber optics and design features of the phototransistor will permit several varieties of logic mixing, modulation, demodulation, and integration functions to be performed. Progressive energization of the fiber optics inputs will produce step functions in the output circuit. This patent combines the inputs of a plurality of fiber optics into a single output signal. However, this prior art patent does not disclose an integrated circuit package.

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L3: Entry 29 of 36

File: USPT

Feb 19, 1980

US-PAT-NO: 4188708

DOCUMENT-IDENTIFIER: US 4188708 A

TITLE: Integrated circuit package with optical input coupler

DATE-ISSUED: February 19, 1980

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Frederiksen; Thomas M.	San Jose	CA		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE	CODE
National Semiconductor Corporation	Santa Clara	CA			02	

APPL-NO: 05/ 953769 [\[PALM\]](#)

DATE FILED: October 23, 1978

## PARENT-CASE:

This is a division of application Ser. No. 839,137, filed Oct. 3, 1977, now U.S. Pat. No. 4,136,357.

INT-CL: [02] B01J 17/00

US-CL-ISSUED: 29/572; 29/589, 264/272, 350/96.15

US-CL-CURRENT: [438/25](#); [257/E23.124](#), [257/E31.118](#), [264/272.17](#), [385/14](#), [438/27](#)

FIELD-OF-SEARCH: 29/588, 29/589, 29/590, 29/572, 264/272

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<a href="#">3694902</a>	October 1972	Afgar	29/588
<input type="checkbox"/>	<a href="#">3968564</a>	July 1976	Springthorpe	29/589
<input type="checkbox"/>	<a href="#">4043027</a>	August 1977	Birchler	29/588

ART-UNIT: 254

PRIMARY-EXAMINER: Tupman; W. C.

ATTY-AGENT-FIRM: Weiss; Harry M.

ABSTRACT:

A plastic encapsulated integrated circuit (IC) package is disclosed which includes a conical depression or dimple precisely located over a photo-responsive semiconductor element incorporated within said integrated circuit for performing a predetermined function. The IC is encapsulated in a clear, two-part epoxy moulding compound preferably Hysol MG-18 having a tapered small depression positioned to register with the photo element but stopping short of actually touching the semiconductor photo element.

Thus, the bottom of the tapered depression consists of a transparent window of sufficient thickness to protect the semiconductor element and still provide optical coupling. The minimum diameter of the light input depression located preferably at the top of the clear plastic package is designed to receive a snug fitting light pipe of Lucite or other clear material that could be used as a fiber optic element. The light pipe can be retained in the IC depression by mechanical means or optionally it can be cemented in place. A suitable light source for activating the photo-responsive semiconductor element in the IC may be a light emitting diode or an incandescent lamp.

5 Claims, 3 Drawing figures

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L3: Entry 36 of 36

File: USPT

Jan 5, 1971

DOCUMENT-IDENTIFIER: US 3553449 A

TITLE: CENTRAL OFFICE CONTROL CIRCUITS FOR REMOTE CONTROL SYSTEMS

CLAIMS:

1. each said input circuit network means including logic elements for combining a plurality of signals, each representing a separate safety check factor related to the selected control function, into a single check signal which actuates said storage means to the selected condition only when the combined safety check signal designates correct conditions for the selected position of that control function; and

c. output circuit means for each storage means electrically coupled to said communication system for actuating the transmission of the selected control function to the remote location only when that associated storage means is in the selected condition.

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L3: Entry 36 of 36

File: USPT

Jan 5, 1971

US-PAT-NO: 3553449

DOCUMENT-IDENTIFIER: US 3553449 A

TITLE: CENTRAL OFFICE CONTROL CIRCUITS FOR REMOTE CONTROL SYSTEMS

DATE-ISSUED: January 5, 1971

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP	CODE	COUNTRY
Hathaway; Homer L.	Penn Hills Township,	Allegheny	County	PA	

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP	CODE	COUNTRY	TYPE	CODE
Westinghouse Air Brake Company corporation of Pennsylvania	ASTX:A	Swissvale	PA				

APPL-NO: 04/ 741729   [\[PALM\]](#)

DATE FILED: July 1, 1968

INT-CL: [] B611 27/00

US-CL-ISSUED: 246/3; 340/163

US-CL-CURRENT: 246/3; 340/3.1, 340/3.7

FIELD-OF-SEARCH: 246/3, 246/135, 246/137, 246/162, 340/163, 340/23

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

[Search Selected](#)   [Search ALL](#)   [Clear](#)

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>3219815</u>	November 1965	Livingston	246/3
<input type="checkbox"/>	<u>3444521</u>	May 1969	Breese	340/163
<input type="checkbox"/>	<u>3452329</u>	June 1969	Pepin	340/163

ART-UNIT: 317

PRIMARY-EXAMINER: La Point; Arthur L.

ASSISTANT-EXAMINER: Libman; George H.

ATTY-AGENT-FIRM: Stout; W. L. Williamson; Arba G.

ABSTRACT:

Remote control system machine circuits incorporating solid state circuitry based on NOR logic. Each control function request is processed through a NOR circuit network which performs suitability checks and conditions a flip-flop element to register, actuate transmission of, and store the requested function. Stored control functions provide within the machine circuits a continuous check of the existing function request for each controlled apparatus at each remote location. A remote location selection network associates the single typical set of control devices with the machine circuits for the location to which selected controls are to be transmitted. Indications of the condition of each item of apparatus at remote stations are received, registered, and displayed by the machine circuits.

10 Claims, 11 Drawing figures

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